Modified Lampert triangle in an organic field effect transistor with traps

K. F. Seidel* and M. Koehler†
Departamento de Física, Universidade Federal do Paraná, C.P. 19044, 81531-990 Curitiba-PR, Brazil
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Applying the surface-charge formalism, we developed a simple theory of trap-filling transitions in organic thin films in a planar field effect transistor geometry. We derived numerical as well as approximate analytical expressions for the current-voltage characteristics and for the saturation current as a function of the gate voltage (saturation transfer curve) in the presence of a discrete set of traps. We show that all single-carrier conduction possibilities in organic field effect transistors with discrete trapping levels are limited within a triangular region of the saturation transfer curve in the logarithmic scale. This region is bounded by the Ohm's law, a trap-free square law, and a trap-filled limit curve which has a voltage threshold and is characterized by a step rise of the saturation current. This "triangle" is equivalent to the Lampert's triangle of the simple space-charge limited conduction theory for one-dimensional charge transport between two Ohmic electrodes. Finally, we show that two of the bounding sides of this triangle were experimentally observed in tetrabenzoporphyrin-based organic field effect transistors reported in the literature [P. B. Shea, J. Kanicki, and N. Ono, J. Appl. Phys. **98**, 014503 (2005)] with the calculated third side fitting the experimental data very well.

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I. INTRODUCTION

The theory of space-charge limited current (SCLC) for bulk conduction between two Ohmic contacts with discrete trapping levels and under constant mobility proposes that all conduction possibilities in an insulator are limited within a triangular region of the current-voltage characteristics (I-V) in the logarithmic scale (Lampert's triangle) bounded by the Ohm's law, Mott-Gurney's trap-free square law, and an essentially vertical trap-filled-limit line.[1–3] The specific location of possible curves within this region depends upon the density and trapping features of a particular localized state, as well as on the thermal-equilibrium free-carrier density in the insulator. In the presence of a single-trap level, all I-V characteristics within the triangular region tend to follow a "modified" Mott-Gurney's square law. This curve has four regimes of conduction: at low voltages the density of injected carriers is lower than the density of free carriers in the insulator and Ohm's law is observed. When the density of injected carriers is greater than the density of free carriers in the insulator, then the current becomes space-charge limited with $I \propto V^2$ (modified Mott-Gurney's square law). In this region the mobility is limited by the traps. At a voltage V_{TFL}, the traps are full and the current rises steeply until it reaches the trap-free space-charge limited regime where the current again depends on the square of the applied voltage (trap-free Mott-Gurney's square law). The value of the trap-filled (TF) limit voltage is $V_{\mathrm{TFL}} \approx eN_t d^2/2\epsilon$, where e is the elementary charge, ϵ is the dielectric constant of the solid, N_t is the density of traps, and d is the length of the insulator. In this paper we show that a similar limiting triangular region, equivalent to the Lampert's triangle, can be established for the saturation current versus the gate voltage in injection-based surface field effect transistors (IFETs).

Contrary to bulk charge transport between two electrodes, trap-filling effects are poorly understood in IFET structures using a film of a high-resistivity semiconductor between source and drain metal electrodes. The operation of such a device involves the injection of a charge-carrier density using a voltage applied between the source and a gate electrode, and the driving of those charges toward the drain using a voltage applied between the source and drain electrodes.[4] Here we call as semiconductor the film of low-conductivity solid that forms the device's active layer, and as insulator the layer that separates this active layer from the gate electrode. Since in general IFETs work in the accumulation regime, the presence of trapping states avoid the buildup of mobile carriers in the active layer with increasing gate voltage (V_g). This effect can significantly influence the magnitude and the shape of current flowing between the source and drain as a function of V_g, especially in the subthreshold region.

A deep understanding of trap-filling effects in IFETs is also needed due to the great technological and fundamental interest in organic field effect transistors (OFETs). OFETs using ordered organic films are essentially IFETs where the active layer is an organic wide-band-gap semiconductor. These materials are characterized by low electric conductivities but room-temperature mobilities in the intermediate range[5,6] so that the OFET operation depends on an efficient injection of carriers from the electrodes. Moreover, it was observed that trapping states in the organic semiconductor induce trap-filling transitions during which the effective-field effect mobility depends strongly on the gate voltage. Several models have been previously proposed to study this phenomena and describe the charge transport in OFETs.[6–12] However, they do not explore the similarities of the trap-filling effects observed in an OFET compared to trap-filling effects observed in a two-electrode device. Some aspects of this relation, such as the identification of a threshold voltage derived from trap filling and a trap-limited square-law regime in the saturation current, were analyzed by Horowitz and Delannoy[13] but to our knowledge, no such general theory of trap-filling effects in organic field effect transistors with discrete trapping levels has been made to date.

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In this paper we present a simple and complete theory of trap-filling effects in IFETs applying a generalization of the surface-charge formalism proposed in a previous work.[14] The advantage of this formalism is that in principle every balance equation relating volumetric densities of trapped and free carriers at each point of the channel can be written using the respective surface charge. One can then carry out a straightforward analogy between the theory of SCLC for a two-electrode device and the charge transport in an IFET structure. However, in IFETs the field produced by the gate voltage generates an accumulation of free carriers near the insulator/semiconductor (I/S) interface. Therefore the steady-state concentrations of free and trapped carriers near the I/S interface is different compared to the concentrations in points far from this interface. This variation in carrier concentrations along the thickness of the semiconductor has to be considered to properly write the balance equations in terms of surface charges. Moreover, the thickness of the accumulation layer also varies along the channel due to the potential difference across the insulator at the source and at the drain.[4] These effects were neglected in Ref. 14 where the steady-state concentrations of free and trapped carriers were assumed uniform throughout the whole thickness of the semiconductor film. Here we propose a simple approach to directly write the balance equations using surface charges while considering, at the same time, the variation in the populations of free and trapped carriers along the semiconductor thickness at each point between the source and drain. This procedure enables us to easily calculate numerically the IFET's characteristic curves, as well as derive analytical approximations for each regime of operation. We show then that all interesting features of the saturation current (I_{sat}) of an IFET are confined within a "triangle" in the $\log I_{sat} \times \log V_g$ plane bounded by the Ohm's law, a trap-free square law, and a trap-filled limit curve that has a threshold voltage and a step current rise. This triangle is the analog for the saturation current in IFETs of the Lampert's triangle.

In the following we present the mathematical formalism together with the assumptions we used to simplify the problem. Initially we applied this formalism to the simple case of one discrete trap level in the semiconductor. Analytical approximations to the *I-V* characteristics and to the variation in the saturation current with the gate voltage (saturation transfer curve) are then derived for each regime of charge transport. Next we extend the formalism to the case of multiple traps and show how to generalize the single trap's analytical approximations to the case of multiple discrete traps. Finally, in Sec. IV we show evidences that two of the bounding sides of the IFET's triangle were measured in a tetrabenzoporphyrin-based OFET reported in the literature.

II. THEORY

A. Assumptions and governing equations

The structure of the IFET we are interested in is schematically depicted in Fig. 1: a thin film of a wide-band-gap semiconductor (the active organic film in OFETs) connects the source and drain contacts, and a high-resistivity gate insulator separates the semiconductor from the gate electrode. In

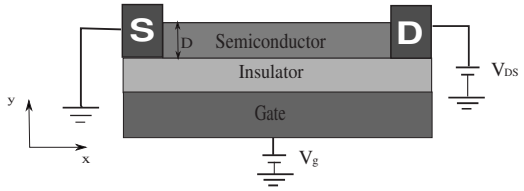

FIG. 1. Schematic view of the injection-based field-effect transistor considered here.

Fig. 1, the direction x measures the distance in the semiconductor from the source electrode and direction y measures the distance in the semiconductor from the gate insulator interface. Since we want to describe the fundamental properties of a model device, several simplifications are considered: (i) We assume a constant, electric-field independent mobility μ. (ii) We neglect diffusion currents. (iii) We use the "gradual channel approximation"[10,14] from which the Gauss equation is separated by associating n_g to dE_y/dy and n_{ds} to dE_x/dx, for n_g and n_{ds}, which are the density of charges injected by the voltage drop between the gate and source/drain electrodes, and by the source-drain voltages, respectively. (iv) We assume that only one type of charge carrier can be injected through Ohmic contacts at the source and drain electrodes. Without loss of generality, we assume that these charge carriers are electrons. The above approximations are necessary to simplify the problem so that it becomes tractable to an elementary mathematical analysis. Yet the simple model that emerges from them is able to describe the main features of the charge transport inside the semiconductor film, allowing quantitative estimations of the essential parameters governing the trap-filling process.

In IFETs the charge-carrier conduction between source and drain is obtained mostly by the flow of free carriers injected from the electrodes. However, we allow for the possibility of (intentional or unintentional) light doping of the semiconductor by considering a constant concentration of free carriers n_0. For an IFET the extrinsic Debye screening length[15,16] associated to n_0, $L_d = \sqrt{kT\epsilon/e^2 n_0}$, satisfies the relation $L_d \gg D$, where D and ϵ are the thickness and the dielectric constant of the semiconductor film, respectively. This relation is the essential condition that characterizes an IFET operation: for a constant n_0 and at low gate voltages, one can show that the thickness necessary to screen the electric field E_y in the semiconductor satisfies the relation $\lambda_0 \propto L_d$.[15] Hence, if the condition $L_d \gg D$ is not satisfied, the action of the field E_y can create an accumulation of free carriers from doping near the I/S interface. In this regime the modulation of the current flow using the gate electrode can be obtained by regulating the thickness and concentration of free carriers in this accumulation layer. As the transistor operation would not depend on carriers injected from the electrodes, the device would resemble a conventional metal-oxide-semiconductor field effect transistor (MOSFET). On the other hand, if the IFET condition is satisfied, n_0 can be considered uniform along the semiconductor thickness. The doping-related surface charge (Q_0) is then independent of the gate voltage and we can write $Q_0 = en_0 D$.

Using the surface-charge notation,[14] the current flow between source and drain is given by

$$\frac{I_{ds}}{W} = [Q_f(x) + Q_0]\mu\frac{dV}{dx}, \tag{1}$$

with W as the channel width, $Q_f(x)$ as the surface charge of free carriers injected from the electrodes, and $V(x)$ as the potential at position x from the source. The introduction of Q_0 in Eq. (1) makes the conductivity between source and drain different from zero when the gate voltage (V_g) is zero.

If L is the distance between source and drain, the integration of Eq. (1) from $x=0$ to $x=L$ gives

$$I_{ds} = \mu\frac{W}{L}\int_0^{V_{ds}} [Q_f(x) + Q_0]dV, \tag{2}$$

where the limits of integration are $V(0)=0$ at the source and $V(L)=V_{ds}$ at the drain.

We assume the presence of multiple trapping states in the semiconductor. For each trap type j, the relation among the total available trap density $N_{t,j}$, the density of occupied traps $n_{t,i}$, and the free-carrier density n_f is given by the balance equation[17] $\partial n_{t,j}/\partial t = \gamma_j n_f[N_{t,j} - n_{t,j}] - \beta_j n_{t,j}$, where γ_j (β_j) is the capture (emission) rate at jth trap level. Assuming steady state between emission and capture at every coordinate x, we find

$$n_{t,j}(x) = \frac{N_{t,j}}{[1 + \delta_j/n_f(x)]}, \tag{3}$$

where $\delta_j = \beta_j/\gamma_j$. δ_j has the units of density and is characteristic of a particular trap level. It decreases with the thermal activation energy of the trap, i.e., its energetic "depth" in the band gap.

Assuming $L \gg D$, n_{ds} can be neglected compared to n_g. n_g is then distributed between the free and the trapped carriers, or

$$n_g(x) = n_f(x) + \sum_j n_{t,j}(x), \tag{4}$$

where the summation over j in Eq. (4) accounts for the presence in the semiconductor of traps with different trapping properties.

Our model is based on the assumption that the injected carrier density is distributed along a characteristic thickness $\ell(x)$ in the y direction. $\ell(x)$ represents the thickness of the accumulation layer. It is very thin in the vicinities of the source (where the field E_y is higher) and becomes thicker on proceeding toward the drain. Using this approximation, we substitute Eq. (3) in Eq. (4) and rewrite the resulting equation in terms of surface-charge densities to find

$$Q_f(x) + Q_f(x)\sum_j \left[\frac{Q_{T,j}}{Q_f(x) + \alpha_j(x)}\right] - Q_g = 0, \tag{5}$$

where $\alpha_j(x) = e\delta_j\ell(x)$ and the surface charges are related to the respective volumetric charge densities by $Q_i(x) = \rho_i\ell(x)$. From the electrostatics, Q_g is a function of V_g and $V(x)$ by the expression $Q_g(x) = C_i[V_g - V(x)]$, where C_i is the gate insulator capacitance per area. Once the variation in ℓ with V is determined, Eq. (5) can be solved to find $Q_f(V)$. Inserting this $Q_f(V)$ in Eq. (2) and performing the numerical integration assuming a constant V_g gives the curve $I_{ds} \times V_{ds}$. The transfer characteristics is obtained following the same procedure but taking V_{ds} constant and changing V_g.

We proceed to obtain a relation among $\ell(x)$, $V(x)$, and V_g. In the y direction the electric field E_y pulls the injected carriers toward the I/S interface. The density of free carriers at this interface builds up until the concentration gradient is sufficient for the resulting diffusion current completely oppose the drift current created by E_y.[4] Neglecting the space-charge generated by trapped carriers, the free charge density of equilibrium[4,10,18] is $\rho(x,y) = 2\epsilon kT/e[y + y_0(x)]^2$, where y_0 represents a characteristic distance from the I/S interface given by

$$y_0(x) = \frac{2\epsilon kT}{e\epsilon_i E_y(x)}, \tag{6}$$

where ϵ_i is the dielectric constant of the insulator. The physical interpretation of y_0 is that half of the charge induced by E_y is within a distance y_0 from the I/S interface.[4] Hence we can assume that $\ell \sim 2y_0$ in Eq. (5). The variation in ℓ with V can be found considering $E_y(x) \sim [V_g - V(x)]/d_i$, where d_i is the thickness of the gate insulator. From Eq. (6) we write

$$V(x) = V_g - \frac{4\epsilon kT}{eC_i\ell(x)}. \tag{7}$$

In Eq. (7), ℓ increases when $V(x) \to V_g$. We thus define the voltage V' so that $\ell = D$ when $V(x) \geq V'$. From Eq. (7), we find $V' = V_g - 4\epsilon kT/eC_iD$. Following Eqs. (6) and (7), the variation in ℓ with $V(x)$ is assumed

$$\ell(x) = \begin{cases} 4\epsilon kT/eC_i[V_g - V(x)] & \text{for } V(x) < V', \\ D & \text{for } V(x) \geq V'. \end{cases} \tag{8}$$

From Eq. (8), the thickness of the accumulation layer is thinner at the source and is given by $\ell_0 = 4\epsilon kT/eC_iV_g$. In the next subsection we will apply this result to derive analytical expressions for I_{ds} for a single-trap level.

B. Analytical approximation for a single-trap level

In this subsection we further simplify our model to consider the case of a single-trap level in the semiconductor layer. Under this assumption, approximate analytical expressions for I_{ds} can be obtained for each regime of charge transport. These expressions are derived taking ℓ_0 as the characteristic thickness of the accumulation layer formed near the I/S interface. Hence, it follows from Eq. (3) that

$$Q_t^0 = \frac{Q_T^0}{1 + (\alpha/Q_f^0)}, \tag{9}$$

where $\alpha = e\delta\ell_0$ and the surface charges are now related to the respective volumetric charge densities by $Q_i^0 = \rho_i\ell_0$.

At very small gate voltages, $Q_f^0 \ll Q_0$ in Eq. (9), and the charge-carrier transport is dominated by the thermal concentration of free carriers (n_0). Integration of Eq. (2) is straightforward and yields

$$I_{ds} = \frac{WD}{L}\mu e n_0 V_{ds}, \tag{10}$$

where we apply the definition of Q_0. The saturation current in this "Ohmic" regime is obtained taking $V_{ds}=V_g$ in Eq. (10) or $I_{\text{sat}}=(WD/L)\mu e n_0 V_g$.

When the density of free carriers injected from the electrodes is higher than n_0 in the accumulation layer, Eq. (10) no longer holds. The charge transport between source and drain is then dominated by the injected carriers. For the trap-limited regime, the majority of the traps are empty so that $\alpha \gg Q_f^0$ in Eq. (9)and Q_t^0 is approximately

$$Q_t^0 \approx \frac{Q_f^0}{\alpha} Q_T^0. \tag{11}$$

From Eq. (4), $Q_g=Q_f^0+Q_t^0$. Substituting Eq. (11) in this relation yields

$$Q_f^0 = Q_g\left(1+\frac{Q_T^0}{\alpha}\right)^{-1}. \tag{12}$$

Introducing Eq. (12) in Eq. (2) and performing the integration gives the I-V characteristics for the trap-limited regime

$$I_{ds} = \frac{W}{L}\mu\left(1+\frac{N_t}{\delta}\right)^{-1} C_i\left[V_g V_{ds} - \frac{V_{ds}^2}{2}\right], \tag{13}$$

where we apply the definitions of Q_T^0 and α. The saturation current is obtained taking $V_{ds}=V_g$ in Eq. (13), which gives

$$I_{\text{sat}} = \frac{W}{2L}\mu\left(1+\frac{N_t}{\delta}\right)^{-1} C_i V_g^2. \tag{14}$$

The product $\mu_{\text{eff}}=\mu[1+(N_t/\delta)]^{-1}$ in Eqs. (13) and (14) represents the effective-field effect mobility of the charge carriers in the trap-limited regime. From this relation one sees that μ_{eff} is lower than μ as it is expected for a trap-limited conduction. Moreover, μ_{eff} does not depend on V_g which produces an increase in the I_{sat} with the square of the gate voltage.

At this point we can determine the gate voltage V_Ω of crossover from Ohm's law to the trap-limited square law in the saturation transfer curve. Equating the saturation currents given by Eqs. (10) and (14), we find $V_\Omega=(Q_0/C_i)[1+(N_t/\delta)]$. Thus V_Ω increases with increasing n_0 or decreasing δ, i.e., higher thermal activation of the trap. At this point, the characteristic curves for the ideal case of a trap-free active layer can be obtained assuming $N_t=0$ in Eqs. (13) and (14). The trap-free square law for the saturation curve is then

$$I_{\text{sat}} = \frac{W}{2L}\mu C_i V_g^2. \tag{15}$$

In the trap-free regime the crossover gate voltage from Ohm's law to the trap-free square law is simply $V_{\text{free}}=Q_0/C_i$.

Upon further increasing the gate voltage in the presence of a single trap, more charges are injected from the electrodes, increasing the density of occupied levels. Eventually, V_g can be high enough to fill all the traps and a TF regime is established in the active layer. Near the TF regime $Q_t^0 \sim Q_T^0$ and, from Eq. (4), $Q_f \approx Q_g - Q_T^0$. Substituting this relation in Eq. (2) and performing the integration gives

$$I_{ds} = \frac{W}{L}\mu C_i\left[(V_g - V_0)V_{ds} - \frac{V_{ds}^2}{2}\right], \tag{16}$$

where $V_0=Q_T^0/C_i=eN_t\ell_0/C_i$. Physically V_0 is the voltage that should be applied to the gate to fill the set of traps with concentration N_t within a distance ℓ_0 from the I/S interface, assuming that all these traps are initially empty. Note that since ℓ_0 depends on V_g V_0 in Eq. (16) changes with the gate voltage.

The saturation current in the TF-limit regime is obtained taking $V_{ds}=V_g-V_0$ in Eq. (16),

$$I_{\text{sat}} = \frac{W}{2L}\mu C_i V_g^2\left(1-\frac{V_0}{V_g}\right)^2. \tag{17}$$

Equation (17) has a strong dependence on the gate voltage when $V_0/V_g \sim 1$. From this condition and the definitions of V_0 and ℓ_0, one finds that there is a steeply rise in the saturation current when the gate voltage approaches the value $V_{\text{TF}}=\sqrt{4\epsilon N_t kT}/C_i$. V_{TF} has the same role for IFETs as the role represented by the trap-filled voltage in the one-dimensional space-charge limited conduction.[13] In the range $V_g \gg V_{\text{TF}}$, I_{sat} tends to the trap-free square law given by Eq. (15).

Figure 2 illustrates a typical saturation transfer curve for a single-trap level in the semiconductor. It was calculated numerically from Eqs. (2) and (5) with $j=1$ and Eq. (8), taking characteristic parameters representative of IFETs using a high-quality organic semiconductor. For comparison, in Fig. 2 we also plot the analytical approximations given by Eq.

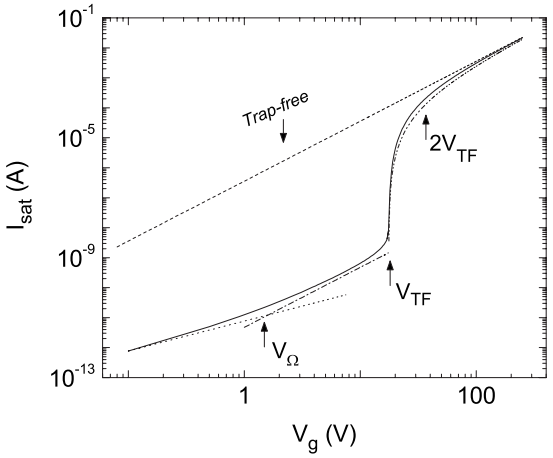

FIG. 2. Saturation current as a function of the gate voltage for a single-trap level. The solid curve is numerically calculated from Eqs. (2), (5), and (8) for $j=1$. The dotted line follows from Eq. (10) with $V_{ds}=V_g$, the dotted-dashed line follows from Eq. (14), and the double-dotted-dashed line follows from Eq. (17). The dashed line follows from Eq. (15) (trap-free regime). The simulation parameters are $L=25$ μm, $W=1.5\times10^{-3}$ m, $D=40$ nm, $C_i=1,2\times10^{-4}$ F/m^2, $\epsilon=3\epsilon_0$, $n_0=2\times10^{17}$ m^{-3}, $\mu=1\times10^{-4}$ m^2/V s, $N_t=10^{25}$ m^{-3}, and $\delta=1.34\times10^{19}$ m^{-3}. The base used in the log $I_{\text{sat}}\times\log V_g$ plot is ten.

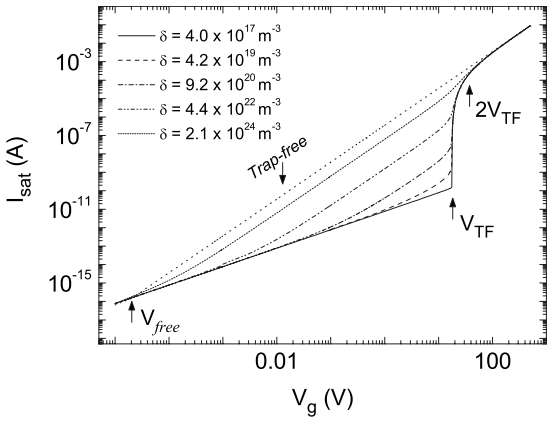

FIG. 3. Saturation current as a function of the gate voltage for trap levels with different thermal activation energies. The curves are numerically calculated from Eqs. (2), (5), and (8) for $j=1$ using the same parameters as in Fig. 2 but with different δ's. The dotted line follows from Eq. (15) (trap-free regime). The base used in the $\log I_{\text{sat}} \times \log V_g$ plot is 10.

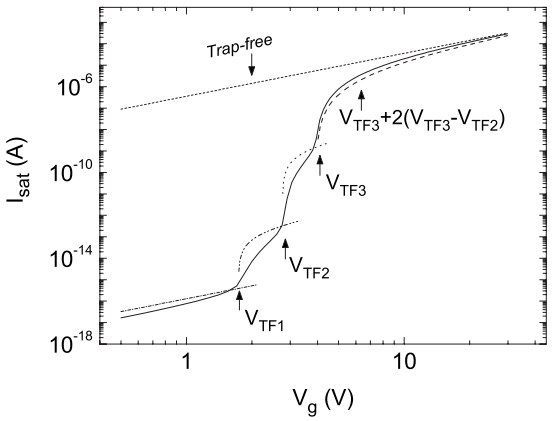

FIG. 4. Saturation current as a function of the gate voltage for three discrete trap levels. The continuous curve is numerically calculated from Eqs. (2), (5), and (8) for $j=3$. The discontinuous curves are analytical approximations. The traps' parameters are $N_{t1}=10^{23}$ m^{-3} and $\delta_1=1.75\times10^{12}$ m^{-3}, $N_{t2}=1.5\times10^{23}$ m^{-3} and $\delta_2=1.84\times10^{15}$ m^{-3}, and $N_{t3}=2.5\times10^{23}$ m^{-3} and $\delta_3=1.34\times10^{19}$ m^{-3}. The other parameters are the same as in Fig. 2. The base used in the $\log I_{\text{sat}} \times \log V_g$ plot is ten.

(10) with $V_{ds}=V_g$ (Ohmic regime), Eq. (14) (trap-limited regime), Eq. (15) (trap-free regime), and Eq. (17) (TF-limit regime), and indicate the values of the characteristic voltages V_Ω and V_{TF}. The solid curve shows four conducting regimes: at low gate voltages the curve increases linearly with V_g up to the gate voltage V_Ω. It then follows a trap-limited square law until the voltage V_{TF} is reached. At V_{TF}, the saturation current rises very steeply with the gate voltage reflecting the huge increase in free carriers available for conduction during the trap-filling transition. The rise in I_{sat} occurs until the density of free carriers in the accumulation layer is $n_f \approx N_t$ at $V_g \sim 2V_{\text{TF}}$. Thereafter the curve tends to the trap-free square-law regime.

From the discussion above we conclude that the same sequence of power-law dependences expected for the *I-V* characteristics of an insulator with a single-trap level sandwiched between two Ohmic contacts[1] is also followed by the saturation current of the IFET. However, we should point out that the physical origin of the square-law dependencies in the two kinds of devices is different: for SCLC conduction the drift velocity of the charge carriers is proportional to the electric field that induces the carrier motion, resulting in a variation in the current with the square of the applied voltage. In the IFETs, the density of free charges induced by the field E_y is proportional to V_g while those charges are drifted toward the drain by the field E_x that, under the saturation condition, is also proportional to V_g. The saturation current is then $I_{\text{sat}} \propto V_g^2$.

Figure 3 shows a family of curves numerically calculated from Eqs. (2), (5), and (8) for the single trap with different values of the parameter δ. The other parameters are the same as those used in calculating the numerical curve in Fig. 2. In Fig. 3 we also plot the trap-free saturation current obtained from Eq. (15). One sees from the curves in Fig. 3 that, with decreasing values of δ (higher thermal activation energies of the trap), the voltage V_Ω approaches V_{TF} and the trap-limited square-law regime is suppressed. The Ohm's law is then observed almost up to the voltage V_{TF}. Beyond this voltage the saturation current follows the trap-filled curve. On the other hand, with increasing values of δ, $V_\Omega \to V_{\text{free}}$ and $\mu_{\text{eff}} \to \mu$. The saturation current approaches then the trap-free square-law regime. Therefore we conclude that for fixed values of n_0 and N_t all important features of the saturation curve are confined within a triangle in the $\log I_{\text{sat}} \times \log V_g$ plane bounded by the Ohm's law given by Eq. (10), the TF-limit curve given by Eq. (17) with a threshold voltage V_{TF}, and the trap-free curve obtained from Eq. (15). We call this triangle a modified Lampert's (ML) triangle in analogy to the similar limiting region proposed by Lampert[1] in the *I-V* characteristics for single-carrier injection in a two-terminal device. From Fig. 3 one also sees that within the ML triangle all curves tend to follow the trap-limited square-law regime.

Using Eqs. (17) and (14) and assuming that at $V_g=2V_{\text{TF}}$, the TF-limit curve approximately merges with the trap-free curve, the ratio of the slopes $\Delta=dI_{\text{sat}}/dV_g$ of the trap-free square-law regime ($\Delta_{\text{T,free}}$), and the slope of the trap-limited curve ($\Delta_{\text{T,limited}}$) at their extrapolate point of intersection[1] is $\Delta_{\text{T,free}}/\Delta_{\text{T,limited}} \sim (1+N_t/\delta)$. Following the same procedure and using Eq. (10) instead of Eq. (17), the ratio between the slope of the trap-free curve and the Ohmic regime ($\Delta_{\text{T,Ohmic}}$) is $\Delta_{\text{T,free}}/\Delta_{\text{T,Ohmic}} \sim (\sqrt{4\epsilon kT/eD})(\sqrt{N_t/n_0})$. The changes in the slope calculated above can be very great which makes the current rise due to trap-filling looks similar to the subthreshold regime of a conventional MOSFET.[13,15]

C. Multiple discrete trap levels

The analysis developed in the previous subsection presents the basic tools in constructing the saturation transfer curve for situations in which there are more than one set of electron traps in the semiconductor. We exemplify the procedure in Fig. 4 using three sets of traps characterized by the densities N_{t1}, N_{t2}, and N_{t3}, respectively, and capture-emission constants δ_1, δ_2, and δ_3, respectively, where $\delta_3 > \delta_2 > \delta_1$ and

$N_{t3} > N_{t2} > N_{t1}$. The continuous line in Fig. 4 plots the transfer curve calculated numerically from Eqs. (2) and (5) with $j=3$ and Eq. (8). The parameters are the same as those used in the simulations of Fig. 2. The current follows a trap-limited square-law regime up to the TF voltage $V_{\mathrm{TF1}} \approx \sqrt{4\epsilon N_{t1} kT/C_i}$. Since the levels with the highest thermal activation energy dominate the charge transport at low gate voltages, the saturation current in this regime can be approximated by Eq. (13) with $\mu_{\mathrm{eff}} = \mu[1+(N_{t1}+N_{t2}+N_{t3})/\delta_1]^{-1}$ and $V_{ds}=V_g$ (dotted-dashed line in Fig. 4). Beyond V_{TF1} the current rises steeply until an injection level such that $n_f \approx N_{t1}$ is reached in the accumulation layer at $V_g \approx 2V_{\mathrm{TF1}}$. Thereafter the curve tends to follow a trap-limited square law up to a voltage $V_{\mathrm{TF2}} \approx V_{\mathrm{TF1}} + \sqrt{4\epsilon N_{t2} kT/C_i}$. In the range $V_{\mathrm{TF1}} < V_g < V_{\mathrm{TF2}}$, the traps with capture-emission constant δ_2 dominate the transport. The saturation current in this region can then be approximated by Eq. (13) with $\mu_{\mathrm{eff}} = \mu[1+(N_{t2}+N_{t3})/\delta_2]^{-1}$ and $V_{ds}=V_g - V_{\mathrm{TF1}}$ (double-dotted-dashed curve in Fig. 4). After V_{TF2} again the current rises steeply until an injection level such that $n_f \approx N_{t1}+N_{t2}$ is reached in the accumulation layer at $V_g \approx V_{\mathrm{TF2}} + 2(V_{\mathrm{TF2}} - V_{\mathrm{TF1}})$. At this point the current tends to follow a trap-limited square law up to the voltage $V_{\mathrm{TF3}} \approx V_{\mathrm{TF2}} + \sqrt{4\epsilon N_{t3} kT/C_i}$. The saturation current in the range $V_{\mathrm{TF2}} < V_g < V_{\mathrm{TF3}}$ region can be approximated by Eq. (13) with $\mu_{\mathrm{eff}} = \mu[1+(N_{t3}/\delta_3)]^{-1}$ and $V_{ds}=V_g - V_{\mathrm{TF2}}$ (dotted curve in Fig. 4). Beyond V_{TF3}, the current rises steeply until an injection level such that $n_f \approx N_{t1}+N_{t2}+N_{t3}$ is reached at $V_g \approx V_{\mathrm{TF3}} + 2(V_{\mathrm{TF3}} - V_{\mathrm{TF2}})$. After this point the current tends to merge with the trap-free square law. In the range $V_g > V_{\mathrm{TF3}}$ the saturation current can be approximated by Eq. (17) with $V_0 = V_{\mathrm{TF3}}$ (dashed curve in Fig. 4). Finally, it is important to note that the trap-filling transition in Fig. 4 starts at V_{TF1} and ends at approximately $V_{\mathrm{TF3}} + 2(V_{\mathrm{TF3}} - V_{\mathrm{TF2}})$ (see Fig. 4). As a consequence, the current rise from the trap-limited square-law regime to the trap-free square-law regime is less abrupt compared to the single-trap transition described in Fig. 2.

III. COMPARISON WITH EXPERIMENTAL DATA

In Fig. 5 we apply our theory to the saturation regime transfer curve measured in an OFET with tetrabenzoporphyrin (TBP) as active layer, and gold as source and drain electrodes.[19] The device was fabricated using a heavily doped n-type silicon wafer that served as mechanical base and gate electrode. The soluble precursor form of TBP was spun cast from the solution onto a 100-nm-thick layer of silicon dioxide to function as the gate insulator ($C_i = 24.5$ nF/cm^2). The precursor is converted into a polycrystalline 120-nm-thick TBP thin film using a process described in Ref. 19. For the device in Fig. 5, $W=12$ mm and $L=22.5$ μm. For simplicity we take the modulus of the negative voltages applied to the injection and conduction of holes in the TBP layer.

From the abrupt rise of the experimental saturation current, we estimate $V_{\mathrm{TF}} \approx 13$ V. It follows from $V_{\mathrm{TF}} = \sqrt{4\epsilon N_t kT/C_i}$ that $N_t = 2.2 \times 10^{25}$ m^{-3}. This value of N_t is two orders of magnitude higher than the density of traps estimated in Ref. 19 using a threshold gate voltage of 17 V.

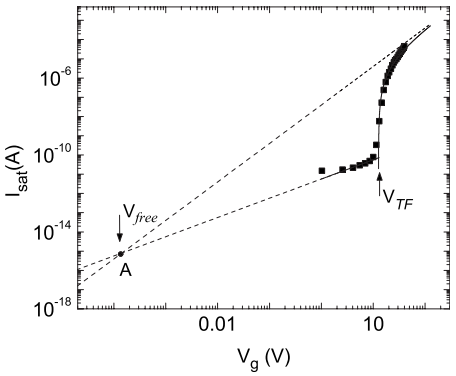

FIG. 5. Transfer saturation curve measured in TBP-based OFET (squares). The solid curves are calculated from Eqs. (10) and (13) with $n_0 = 9 \times 10^{17}$ m^{-3}, $\mu = 6.1 \times 10^{-6}$ m^2/V s, and a threshold voltage given by V_{TF} with $N_t = 2.2 \times 10^{25}$ m^{-3}. The theoretical voltage to the trap-free regime (V_{free}) is defined at point A of the Ohm's law and a line with slope 2 is extended from point A to high gate voltages. This line represents the trap-free regime. The base used in the log $I_{\mathrm{sat}} \times$ log V_g plot is ten.

The difference comes from the assumption in Ref. 19 that all the traps along the thickness of the semiconductor film are homogeneously filled by the injected charge. Hence the authors in Ref. 19 approximated V_{TF} by $V_{\mathrm{TF}} \approx eN_t D/C_i$. This assumption is obviously not precise, especially for thick devices, since the electrostatic action of the gate induces a higher concentration of filled states within a characteristic thickness approximately equal to ℓ_0 from the semiconductor/insulator interface. Therefore, the estimation of N_t using the procedure of Ref. 19 underestimates the density of traps by a multiplicative factor of order $\approx D/\ell_0$ compared to our procedure (for instance, when $V_g = 17$ V, $\ell_0 \approx 1$ nm which gives $D/\ell_0 \approx 120$).

The theoretical curves (solid lines in Fig. 5) are from Eqs. (10) and (13) using adjustable n_0 and μ, and a threshold voltage given by $V_{\mathrm{TF}} = 13$ V. From fitting we obtain $n_0 = 9 \times 10^{17}$ m^{-3} and $\mu = 6.1 \times 10^{-7}$ m^2/V s. Our μ is in the range of values measured in Ref. 19 for the field effect mobility of holes in TBP devices, between 3.6×10^{-7} and 1.1×10^{-6} m^2/V s. It is important to note that the values of n_0 and μ above are obtained in order to give a self-consistent trap-free line:[20] from $V_{\mathrm{free}} = en_0 D/C_i$, and for a given value of n_0, we calculate V_{free}. This voltage defines the point A in the extrapolation of the Ohm's law to lower gate voltages in the log $I_{\mathrm{sat}} \times$ log V_g plane (see Fig. 5). Then from this point we extend a line with slope 2 to higher gate voltages which represents the trap-free curve. The self-consistent values of n_0 and μ are those which fit the experimental data and simultaneously merge the trap-filled curve calculated from Eq. (13) with the line extended from point A in the range of high V_g. Using this procedure one sees that all experimental points in Fig. 5 are within the triangular region of the log $I_{\mathrm{sat}} \times$ log V_g plane limited by the trap-free curve, the Ohm's law curve, and the TF-limited curve. This result suggests that the data measured in the TBP-based OFET represent two of the bounding sides of a ML triangle.

At high gate voltages, the experimental data in Fig. 5 apparently tends to merge with trap-free curve. Hence there

appears to be no room for further trap-filling transition within the ML triangle. This result is consistent with measurements in alpha-sexithienyl (α6 T) OFETs where the charge transport was modeled using a single dominant trap level.[13] In α6 T a trap-limited square-law regime is apparent in the measurements (here we mention we have also applied our model to fit the data shown in Fig. 9 of Ref. 13, reproducing nicely the transition from the trap-limited to the trap-filled square-law regimes observed in the α6 T device). In TBP, however, the Ohm's law is observed almost up to V_{TF} which suggests high thermal activation energy in relation to the main transport states. Since the trap-limited square-law regime is not apparent in the TBP experimental curve, we assume a value of δ so that $V_{\Omega}=V_{\mathrm{free}}$ for $N_t=2.2\times10^{25}$ m^{-3}, which yields $\delta=3.8\times10^{19}$ m^{-3}. Using this result and assuming that δ is related to the density of conducting states (N_c) and the thermal activation energy of the trap (E_a) by $\delta=N_c\exp(-E_a/kT)$,[13] we can estimate $E_a\sim0.38$ eV for $N_c=10^{26}$ m^{-3}.[13] This energy is deeper compared to the activation energy of the dominant level in α6 T which is $E_a\sim0.23$ eV.[13]

The last point to be considered is the relation between the extrinsic Debye screening length and the thickness of the TBP film. From the definition of the extrinsic Debye screening length and taking the value of n_0 above, we have $L_d\sim2.2$ μm at $T=300$ K. Since $D=120$ nm, $L_d/D\sim18$ which reasonably satisfy the IFET condition.

IV. CONCLUSION

Using a simple theory to model trap-filling transitions in organic field effect transistors, we identified a triangular region in the saturation transfer curve plotted in the logarithmic scale that confines all conduction regimes for the charge transport in this kind of devices when discrete sets of trapping states are present. This triangle is limited by the Ohm's law, a trap-free square law, and the trap-filled limit line characterized by a step rise of the saturation current after a threshold gate voltage.

Considering the single-trap case, we derived analytical expression for the *I-V* characteristics and the saturation current as a function of the gate voltage for each regime of charge transport. We show that all particular single-trap saturation transfer curves within the modified Lampert's triangle tends to follow a trap-limited square-law regime where the effective-field effect mobility depends on the trap's density and energetic depth relative to the main conducting states. We numerically calculated the saturation transfer curve when multiple sets of traps are present in the active layer and demonstrated how the analytical expressions for single traps can be applied to reproduce the main features of this curve. In this case the presence of multiple trap-filling transitions very close in voltage decreases the steepness of the saturation current rise with increasing gate voltage compared to the single-trap case.

Finally, we applied our theory to fit the experimental saturation transfer curve measured in OFETs based on a thin film of TBP. We found good agreement between theory and experiment. The absence of a clear trap-limited square-law regime in these measurements suggests that the data correspond to the observation of two of the bounding sides of the modified Lampert's triangle for IFETs.

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*keli@fisica.ufpr.br
†koehler@fisica.ufpr.br

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